REMARKS

Claims 2 to 7 are pending in the above-identified application. Claim 2 is independent.

Summary of the Present invention

The present invention is directed to a high-frequency multilayer circuit substrate used in a microwave band. The invention has as an objective to provide a multilayer circuit substrate capable of executing low-reflection low-loss inter-circuit-layer transmission with a simple structure and reduced manufacturing cost.

In an embodiment of the present invention, a plurality of circuit layers are connected to each other by a via hole, and the impedance of the via hole connecting portion matches the impedance of the signal transmission line by way of a planar impedance matching circuit forming a connection between the via hole and the signal transmission line. Thus, matching the impedance of the via hole connecting portion to the impedance of the signal transmission line only requires adjusting the width and length of the impedance matching transmission line.

Alternatively, an impedance matching portion is formed by the impedance matching transmission line and stubs connected to both sides of the transmission line at an end closest to the signal transmission line. The impedance is controlled by adjusting the width and length of the impedance matching transmission line and the width and length of each of the stubs.

In a further embodiment, an impedance matching circuit is formed by a plurality of planar impedance matching transmission lines having at least two different widths. The impedance is controlled by adjusting the widths and lengths of the impedance matching transmission lines.

Thus, Applicants have developed a structure having low manufacturing costs. Further, Applicants have determined that based on such a simple planar structure requiring only adjustment of the width and height of impedance matching transmission lines, a low transmission loss and a reduction in reflection loss can be achieved at a high frequency of about 60GHz (see Figures 5 and 10). Thus, the present invention is particularly suitable for millimeter band signal transmission.

Claim Objection

The claims have been object to because of the word "plane." Accordingly, Applicants have replaced the word "plane" with –planar, throughout the claims, as recommended, as well as throughout the Specification.

Claim Rejection – 35 U.S.C. 112

Claims 4 and 5 have been rejected due to a lack of clarity of the phrase "at the other end thereof." Applicants have amended that phrase to define that the other end is the one connected to the signal transmission line (as was recited in original claim 2). Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim Rejections – 35 U.S.C. 102

Claims 1-3 have been rejected under 35 U.S.C. 102(b) as being anticipated by Eda et al. (U.S. Patent 5,387,888, hereinafter Eda). By this Amendment, claim 2 has been re-written into independent form and claim 1 has been canceled. Applicants respectfully traverse this rejection.

Claim 2 is directed to a high-frequency multilayer circuit substrate, which among other things includes a planar impedance matching circuit formed by an impedance matching transmission line, one end of which is connected to the via hole and other end of which is connected to the signal transmission line. Applicants submit that Eda does not teach or suggest at least that claimed limitation.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385 388 (Fed. Cir.); cert. Dismissed, 468 U.S. 1228 (1984); W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. Denied, 469 U.S. 851 (1984).

Eda is directed to high-frequency ceramic multi-layer substrate (see, for example, Figure 5) having an embedded stripline 221 connected to an electric circuit 209 through via holes 224, 225, by way of a stripline 201. Eda's stripline 221 does not connect the via holes 224, 225 to a signal transmission line, e.g. 201. Eda's stripline 201 also does not connect a signal transmission line to the via

holes 224, 225. Thus, Applicants submit that Eda does not disclose all claimed elements of claim 2. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claims 1-3 have been rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa et al. (U.S. Patent 5,717,249, hereinafter Yoshikawa). For reasons comparable to the above rejection based on Eda, Applicants respectfully traverse this rejection.

Yoshikawa is directed to a plurality of ceramic substrates stacked in layers to form a multilayer structure. An RF impedance matching circuit 8 is formed on the first ceramic substrate. On the uppermost layer of the multilayer structure, characteristics of the RF matching circuit can be adjusted such that a RF power amplifying circuit device can be used in a frequency range of 100 MHz or more (Yoshikawa at column 7, lines 33-47). Characteristics of the RF impedance matching circuit can be adjusted by trimming (column 7, lines 49-53). Unlike the claimed invention, however, Yoshikawa's RF impedance matching circuit does not connect a via hole to a signal transmission line. Thus, Applicants submit that Yoshikawa does not disclose all claimed elements of claim 2. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim Rejections – 35 U.S.C. 103

Claims 4 and 5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Eda. In the alternative, claims 4 and 5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa. Applicants respectfully traverse these rejections.

At least for the reasons above for claim 2, Applicants submit that Eda, or Yoshikawa, do not teach or suggest all claimed elements of claims 4 and 5, as well. Furthermore, the Office Action admits that each of the references do not disclose a stub on each side of an impedance matching line. Instead, the Office Action alleges that such a limitation is a mere optimization of impedance matching. Applicants submit, however, that the present invention is a simpler structure than the structures disclosed in either of the references. Applicants structure results in an easier manufacturing process for a device that can achieve frequencies in the millimeter band, with reduced transmission and reflection losses. Thus, at least for these reasons the rejections fail to establish *prima facie* obviousness of claims 4 and 5. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claims 6 and 7 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Eda in view of Okada et al. (U.S. Patent 5,701,128, hereinafter Okada). In the alternative, claims 6 and 7 have been rejected under 35 U.S 103(a) as being unpatentable over Yoshikawa in view of Okada. Applicants respectfully traverse these rejections.

At least for the same reason as above for claim 2, Applicant submits that all claimed elements are not taught or suggested for claims 6 and 7, as well. Furthermore, the Office Action relies on Okada for disclosing stubs connected to transmission lines is functionally equivalent to lines having different widths connected in series. Applicants submit that Okada does not make up for the deficiency in Eda of not teaching or suggesting an impedance matching line which

connects a via hole to a signal transmission line. Similarly, Applicants submit that Okada does not make up for the deficiency in Yoshikawa of not teaching or suggesting an impedance matching circuit connecting a via hole to a signal transmission line. Accordingly, Applicants submit that at least for these additional reasons, the rejections fail to establish *prima facie* obviousness for claims 6 and 7. Applicants respectfully request that the rejection be withdrawn.

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

(Rev. 02/20/02)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning on page 6, line 15, has been amended as follows:

Taking high-frequency characteristics of a via hole into consideration, the present inventor discovered a method for eliminating signal wave reflection in the via hole connecting portion and a transmission loss due to the reflection by regarding the via hole as a circuit component having a characteristic impedance different from that of a signal transmission line and by providing an adjustable impedance matching [plane] planar circuit between the via hole and the signal transmission line.

The paragraph beginning on page 9, line 3, has been amended as follows:

A [plane] planar impedance matching circuit is constructed of the rectangular stubs 303 and the impedance matching microstrip line 304. A via hole connecting portion is constructed of the via hole 110, the via hole metal pad 102, the via hole metal pad 202, the via hole metal pad 302, the rectangular stubs 303 and the impedance matching microstrip line 304.

The paragraph beginning on page 10, line 5, has been amended as follows:

Fig. 5 shows the decibel value of reflection loss (S11) and the decibel value of transmission loss (S21) in the case where the length of the impedance matching microstrip line 304 (shown in Fig. 4) is 180 μm and the length of the rectangular stubs 303 (shown in Fig. 4) is 100 μm. For the sake of comparison, Fig. 6 shows a

transmission characteristic in the case where no [plane] planar impedance matching circuit is provided. In Fig. 5 and Fig. 6, the horizontal axis represents frequency, while the vertical axis represents the reflection loss and the transmission loss.

The paragraph beginning on page 12, line 22, has been amended as follows:

A [plane] planar impedance matching circuit is constructed of the impedance matching microstrip lines 404 and 405. A via hole connecting portion is constructed of the via hole 410, via hole metal pad 402, via hole metal pad 502, via hole metal pad 602 and impedance matching microstrip lines 404 and 405.

The paragraph beginning on page 14, line 16, has been amended as follows:

Furthermore, in the aforementioned first and second embodiments, the characteristic impedance of the via hole connecting portion is matched to the characteristic impedance of the microstrip transmission line to which the via hole connecting portion is connected and which is served as the signal transmission line. However, it is acceptable to match the characteristic impedance of the via hole connecting portion with the characteristic impedance of a [plane] planar circuit that is connected directly to the via hole connecting portion through no signal transmission line.

The paragraph beginning on page 15, line 1, has been amended as follows:

As is apparent from the above, according to the high-frequency multilayer circuit substrate of the present invention, the characteristic impedance of the via hole connecting portion, which is constructed of the via hole and the [plane] planar

circuit, can be matched to the characteristic impedance of the transmission line with a simple structure in terms of design and manufacturing. As a result, low-reflection low-loss inter-circuit-layer transmission in a microwave region, particularly in the millimeter wave region, can be achieved with a simple structure, allowing the manufacturing cost to be reduced. Furthermore, this high-frequency multilayer circuit substrate can be effectively utilized for the development of circuits and packages in the microwave region, particularly in the millimeter wave region.

IN THE CLAIMS:

Claim 1 have been canceled.

The claims have been amended as follows:

2. (Amended) A high-frequency multilayer circuit substrate [as set forth in claim 1, wherein] comprising:

a plurality of circuit layers;

a via hole penetrating the plurality of circuit layers to be connected to each other;

a planar impedance matching circuit connected to the via hole; and

a signal transmission line connected to the planar impedance matching circuit, wherein

a characteristic impedance of a via hole connecting portion formed by the via hole and the planar impedance matching circuit matches a characteristic impedance of the signal transmission line,

the planar impedance matching circuit is formed by an impedance matching transmission line, one end of which is connected to the via hole and other end of which is connected to the signal transmission line.

3. (Amended) A high-frequency multilayer circuit substrate as set forth in claim 2, wherein

the characteristic impedance of the via hole connecting portion [is matched to] matches the characteristic impedance of the signal transmission line based on an adjusted [by adjusting a] width and [a] length of the impedance matching transmission line.

4. (Amended) A high-frequency multilayer circuit substrate as set forth in claim 2, wherein

the [plane] planar impedance matching circuit is formed by the impedance matching transmission line and stubs which are connected to both sides of the impedance matching transmission line at the other end [thereof] connected to the signal transmission line.

5. (Amended) A high-frequency multilayer circuit substrate as set forth in claim 4, wherein

the characteristic impedance of the via hole connecting portion [is matched to] matches the characteristic impedance of the signal transmission line based on an adjusted [by adjusting the] width and [the] length of the impedance matching transmission line and a width and a length of each of the stubs.

6. (Amended) A high-frequency multilayer circuit substrate as set forth in claim 2, wherein

the [plane] planar impedance matching circuit is formed by a plurality of impedance matching transmission lines having at least two different widths and connected in series to the via hole and the signal transmission line.

7. (Amended) A high-frequency multilayer circuit substrate as set forth in claim 6, wherein

the characteristic impedance of the via hole connecting portion [is matched to] matches the characteristic impedance of the signal transmission line [by adjusting] based on adjusted widths and lengths of the impedance matching transmission lines.